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10/736,852	12/16/2003	Joseph J. Nahas	SC13123TC	6904

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EXAMINER	
LAMARRE, GUY J	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/736,852	NAHAS, JOSEPH J.	
	Examiner	Art Unit	
	Guy J. Lamarre	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/19/06*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

NON-FINAL OFFICE ACTION

* This office action is in response to Applicants' submission of *10/19/06*.

1. **Claims 1-27** remain pending.

1.1 The indicated allowability of **Claims 1-27** of record is withdrawn in view of newly found (US PGPub No. 2003/0023928) to **Jedwab et al.;** (US Patent No. 6,704,230) to **DeBrosse et al.;** (US Patent No. 6,584,589) to **Perner et al.** The delay in citation of such references is regretted. The rejection to these Claims based on some of the newly discovered prior art references is as follows.

Claim Rejections - 35 USC ' 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

.1 **Claims 1-27** are rejected under 35 U.S.C. 102 (e) as being anticipated by (US Patent No. 6,704,230) to **DeBrosse et al.**

As per Claims 1-27, DeBrosse et al. anticipates the claimed invention because Fig. 2 depicts an error counter (block 265) for memory core (block 230) for logging errors occurring subsequent to detection/ECC (block 220) thereof via testing memory access through a magnetoresistive random access memory (MRAM) core, e.g., '*Counters can be used as well, as depicted in FIG. 2. For example, as shown in FIG. 2, the ECC processor (220) can update an error counter to cause the storage area to be refreshed after a particular number of errors has been detected, or, alternatively, when a particular number of errors has not been detected. In addition, there are intervals when no write operations are performed to a particular MRAM or sub-array of the MRAM, for example, when the storage area is either inactive or only read from*

time to time. In such intervals in which no write operations are being performed, a refresh operation can be omitted for the MRAM or the sub-array.'

Fig. 2 depicts memory access (block 210) comprising: a read operation, a compare operation, and a write operation, toggle operation effected in accordance with memory access cycle time.

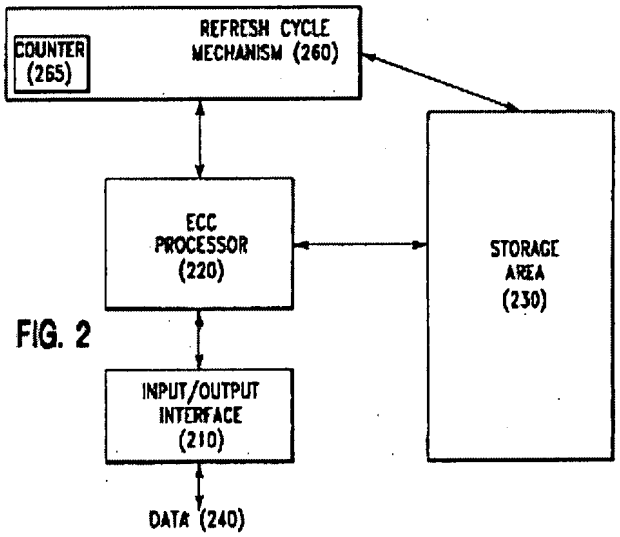

FIG. 2

As per Claims 1-2, 8-9, 18-19, DeBrosse et al. discloses, in Fig. 2, the claimed memory circuit, comprising: a magnetoresistive random access memory (MRAM) core for storing data received by the memory circuit and outputting stored data, the magnetoresistive random access memory (MRAM) having a reserved portion; an error correction code (ECC) coder for adding a redundancy code to the data for storing in the magnetoresistive random access memory (MRAM) core; an ECC (BLOCK 220) corrector, coupled to the magnetoresistive random access memory (MRAM) core, for performing an analysis of the stored data and the redundancy code to detect and correct errors in the stored data that is output by the magnetoresistive random access memory (MRAM) core and providing an error signal when an error is detected from the analysis; and an error counter, coupled to the ECC (BLOCK 220) corrector and the magnetoresistive

random access memory (MRAM) core, for providing a count of occurrences of the error signal for storage in the reserved portion of the magnetoresistive random access memory (MRAM) core.

As per Claim 3, DeBrosse et al. discloses, in Fig. 2, the claimed memory circuit of claim 1, further comprising a write cycle counter (block 265) for providing a count of occurrences of writing data in the magnetoresistive random access memory (MRAM) core for storage in the reserved portion of the magnetoresistive random access memory (MRAM) core.

As per Claim 4, DeBrosse et al. discloses, in Fig. 2, the claimed memory circuit of claim 3, further comprising a read cycle counter (block 265) for providing a count (block 265) of occurrences of reading data from the magnetoresistive random access memory (MRAM) core for storage in the reserved portion of the magnetoresistive random access memory (MRAM) core.

As per Claim 5, DeBrosse et al. discloses, in Fig. 2, the claimed memory circuit of claim 4, wherein the read cycle counter (block 265) and the write cycle counter (block 265) are coupled to the magnetoresistive random access memory (MRAM) core by the ECC (BLOCK 220) coder.

As per Claim 6, DeBrosse et al. discloses, in Fig. 2, the claimed memory circuit of claim 1, further comprising control means for initiating writing the count (block 265) of the error counter (block 265) during an end portion of a read cycle and completing writing the count (block 265) of the error counter (block 265) ,before or during a beginning portion of a cycle immediately following the read cycle.

As per Claim 7, DeBrosse et al. discloses, in Fig. 2, the claimed memory circuit of claim 6, wherein the control means causes performance of a read operation (block 210), a compare operation (block 210), and a toggle operation (block 210) to perform a write cycle.

As per Claim 8. A memory circuit, comprising: a non-volatile random access memory

(NVRAM) core for storing data received by the memory circuit and outputting stored data; an ECC (BLOCK 220) corrector, coupled to the non-volatile random access memory (NVRAM) core, for performing an analysis of stored data fetched from the non-volatile random access memory (NVRAM) core during a read cycle of the non-volatile random access memory (NVRAM) core to detect and correct errors in the stored data that is output by the non-volatile random access memory (NVRAM) core and providing an error signal when an error is detected from the analysis; and an error counter, coupled to the ECC (BLOCK 220) corrector and the non-volatile random access memory (NVRAM) core, for providing a count (block 265) of occurrences of the error signal for storage in the non-volatile random access memory (NVRAM) core.

As per Claim 9, DeBrosse et al. discloses, in Fig. 2, the claimed memory circuit of claim 8, further comprising an ECC (BLOCK 220) coder, coupled to the non-volatile random access memory (NVRAM) core, for adding a redundancy code to the data for storing in the non-volatile random access memory (NVRAM) core.

As per Claim 10, DeBrosse et al. discloses, in Fig. 2, the claimed memory circuit of claim 9, wherein the ECC (BLOCK 220) corrector is further characterized as performing an analysis of the redundancy code to detect and correct errors.

As per Claim 11, DeBrosse et al. discloses, in Fig. 2, the claimed memory circuit of claim 10, wherein the non-volatile random access memory (NVRAM) core has a reserved portion and the count (block 265) of the error counter (block 265) is stored in the reserved portion.

As per Claim 12, DeBrosse et al. discloses, in Fig. 2, the claimed memory circuit of claim 9, wherein the error counter (block 265) is coupled to the non-volatile random access memory (NVRAM) core by the ECC (BLOCK 220) coder.

As per Claim 13, DeBrosse et al. discloses, in Fig. 2, the claimed memory circuit of claim 9,

further comprising a write cycle counter (block 265) for providing a count (block 265) of occurrences of writing data in the non-volatile random access memory (NVRAM) core for storage in the non-volatile random access memory (NVRAM) core.

As per Claim 14, DeBrosse et al. discloses, in Fig. 2, the claimed memory circuit of claim 13, further comprising a read cycle counter (block 265) for providing a count (block 265) of occurrences of reading data from the non-volatile random access memory (NVRAM) core for storage in the non-volatile random access memory (NVRAM) core.

As per Claim 15, DeBrosse et al. discloses, in Fig. 2, the claimed memory circuit of claim 14, wherein the read cycle counter (block 265) and the write cycle counter (block 265) are coupled to the non-volatile random access memory (NVRAM) core by the ECC (BLOCK 220) coder.

As per Claim 16, DeBrosse et al. discloses, in Fig. 2, the claimed memory circuit of claim 8, wherein the non-volatile random access memory (NVRAM) core is a magnetoresistive random access memory core, and further comprises control means for initiating writing the count (block 265) of the error counter (block 265) during an end portion of a read cycle and completing writing the count (block 265) of the error counter (block 265) before or during a beginning portion of a cycle immediately following the read cycle.

As per Claim 17, DeBrosse et al. discloses, in Fig. 2, the claimed memory circuit of claim 16, wherein the control means causes performance of a read operation (block 210), a compare operation (block 210), and a toggle operation (block 210) to perform a write cycle.

As per Claim 18. A method of operating a memory circuit having a non-volatile random access memory (NVRAM) core, comprising: storing data received by the memory circuit in the non-volatile random access memory (NVRAM) core; outputting the data stored in the non-volatile random access memory (NYRAM) core; performing an analysis of the data output from the non-volatile random access memory (NVRAM) core to detect and correct errors therein; obtaining a

count (block 265) of detected errors; and storing the count (block 265) in the non-volatile random access memory (NVRAM) core.

As per Claim 19, DeBrosse et al. discloses, in Fig. 2, the claimed method of claim 18, further comprising: storing a redundancy code with the data in the non-volatile random access memory (NVRAM) core.

As per Claim 20, DeBrosse et al. discloses, in Fig. 2, the claimed method of claim 19, wherein the performing the analysis further comprises analyzing the redundancy code.

As per Claim 21, DeBrosse et al. discloses, in Fig. 2, the claimed method of claim 20, wherein storing the count (block 265) further comprises: initiating the storing of the count (block 265) during an end portion of a next read cycle of the memory circuit after an error has been detected; and completing the storing of the count (block 265) before or during an initial portion of a cycle immediately following the next read cycle.

As per Claim 22, DeBrosse et al. discloses, in Fig. 2, the claimed method of claim 21 further comprising implementing the non-volatile random access memory (NVRAM) core as a magnetoresistive random access memory core and implementing the cycle immediately following the next read cycle as a write cycle, wherein, the write cycle comprises a read operation (block 210), a compare operation (block 210), and a toggle operation (block 210).

As per Claim 23, DeBrosse et al. discloses, in Fig. 2, the claimed method of claim 18 further comprising implementing the non-volatile random access memory (NVRAM) core with bit cells having storage values that are changed by toggling their state.

As per Claim 24, DeBrosse et al. discloses, in Fig. 2, the claimed method of claim 18, further comprising: obtaining a count (block 265) of read cycles; storing the count (block 265) of read cycles in the non-volatile random access memory (NVRAM) core; obtaining a count (block 265) of write cycles; and storing the count (block 265) of write cycles in the non-volatile random

access memory (NVRAM) core.

As per Claim 25, DeBrosse et al. discloses, in Fig. 2, the claimed method of claim 24, further comprising: comparing the count (block 265) of detected errors to the count (block 265) of write cycles.

As per Claim 26, DeBrosse et al. discloses, in Fig. 2, the claimed method of claim 24, further comprising: comparing the count (block 265) of detected errors to the count (block 265) of read cycles.

As per Claim 27, DeBrosse et al. discloses, in Fig. 2, the claimed method of claim 24, further comprising: comparing the count (block 265) of detected errors to a sum of the count (block 265) of read cycles and the count (block 265) of write cycles.

.2 Claims 1-2, 8-9, 18-19, are rejected under 35 U.S.C. 102 (e) as being anticipated by (US Patent No. **6,584,589**) to **Perner et al.**

As per Claims 1-2, 8-9, 18-19, Perner et al. anticipates the claimed invention because Fig. 1 depicts an error counter (e.g., block 101) for memory core (block 102) for logging/marking errors occurring subsequent to detection/ECC (e.g., block 108) thereof via testing memory access through a magnetoresistive random access memory (MRAM) core, e.g., *'Errors reported by the column test circuits may be single bit errors that are correctable by ECC (Error Correction Circuits) or may be multiple bit errors that warrant the row being marked as a `BAD` row. A counter is used to determine whether there are a sufficient number of errors for marking the row `BAD`. If the column error flag indicates an error condition exists, the data in the sense amplifier data I/O scan registers is shifted into the column error counter (110 in FIG. 1). When the row error count exceeds a value determined as un-correctable by an external ECC, the row may be marked as `BAD`. Error data created by the built-in self test circuits may be collected by external circuits for future processing or reported to the tester. One external circuit*

to hold the built-in self test data is a `status register` that would be used by the system using the MRAM to direct the writing of data into known good memory locations.

... The preferred implementation of the present invention involves several integrated built-in test circuits that can be used to perform a comprehensive set of tests to locate defects in a MRAM memory array. Shorted elements and open rows can be detected with the use of row wired-OR test circuit. Dynamic Hi/Lo memory cell resistance tests are carried out through the use of specially constructed sense amplifier circuits. Pattern tests can be performed with the use of exclusive-OR circuits integrated into the sense amplifiers and using the scan data I/O registers. Outputs from the Hi/Lo and pattern tests examine the performance of individual MRAM memory elements. A wired-OR circuit is used to combine the Hi/Lo and pattern tests results into a single column error flag. If the column error flag is set, an error test counter is included to count the number of cells in a row the are marked as BAD. The column error count may be used to determine if the row of data is ECC correctable.'

Fig. 1 depicts memory access (row/column address) comprising: a read operation, a compare operation, and a write operation, toggle operation effected in accordance with memory access cycle time.

As per Claims 1-2, 8-9, 18-19, Perner et al. discloses, in Fig. 1, the claimed memory circuit, comprising: a magnetoresistive random access memory (MRAM) core for storing data received by the memory circuit and outputting stored data, the magnetoresistive random access memory (MRAM) having a reserved portion; an error correction code (e.g., block 108) coder for adding a redundancy code to the data for storing in the magnetoresistive random access memory (MRAM) core; an ECC (e.g., block 108) corrector, coupled to the magnetoresistive random access memory (MRAM) core, for performing an analysis of the stored data and the redundancy code to detect and correct errors in the stored data that is output by the

magnetoresistive random access memory (MRAM) core and providing an error signal when an error is detected from the analysis; and an error counter, coupled to the ECC (e.g., block 108) corrector and the magnetoresistive random access memory (MRAM) core, for providing a count of occurrences of the error signal for storage in the reserved portion of the magnetoresistive random access memory (MRAM) core

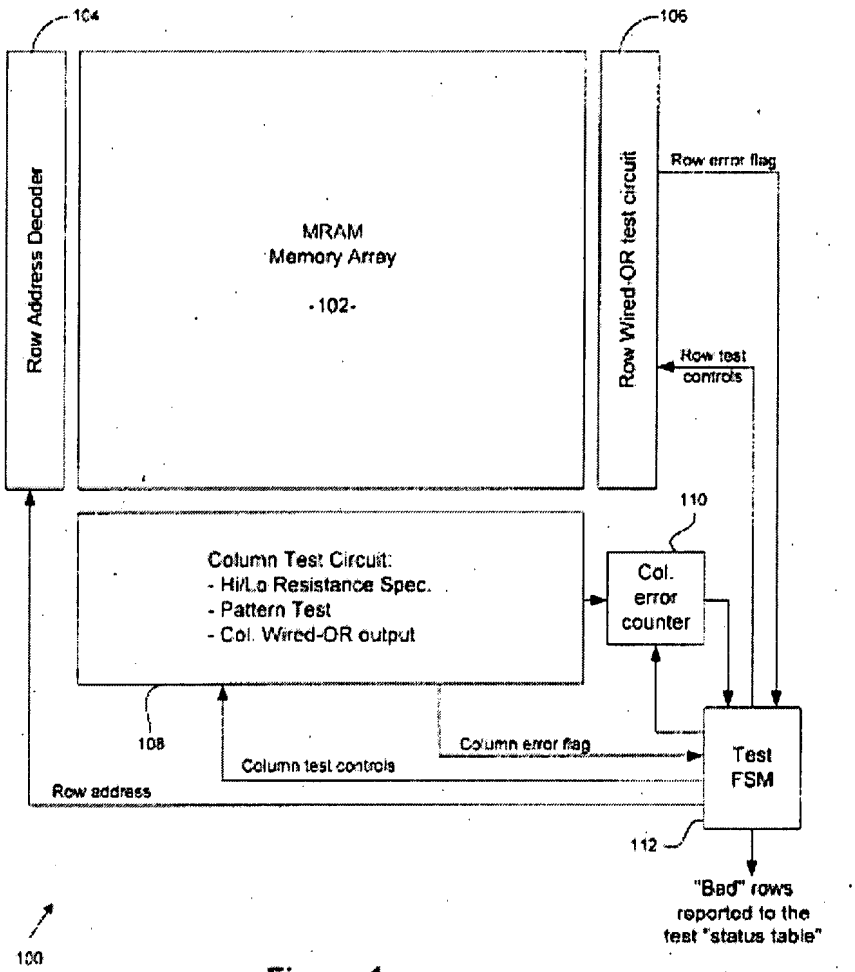

Figure 1

CONCLUSION

* Any response to this action should be mailed to:

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or faxed to: (571) 273-8300 for all formal communications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (571) 272-3826. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques, can be reached at (571) 272-6962.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-3609.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Guy J. Lamarre, P.E
Primary Examiner